IAP22
JUN 30 2006
PATENT & TRADEMARK OFFICE

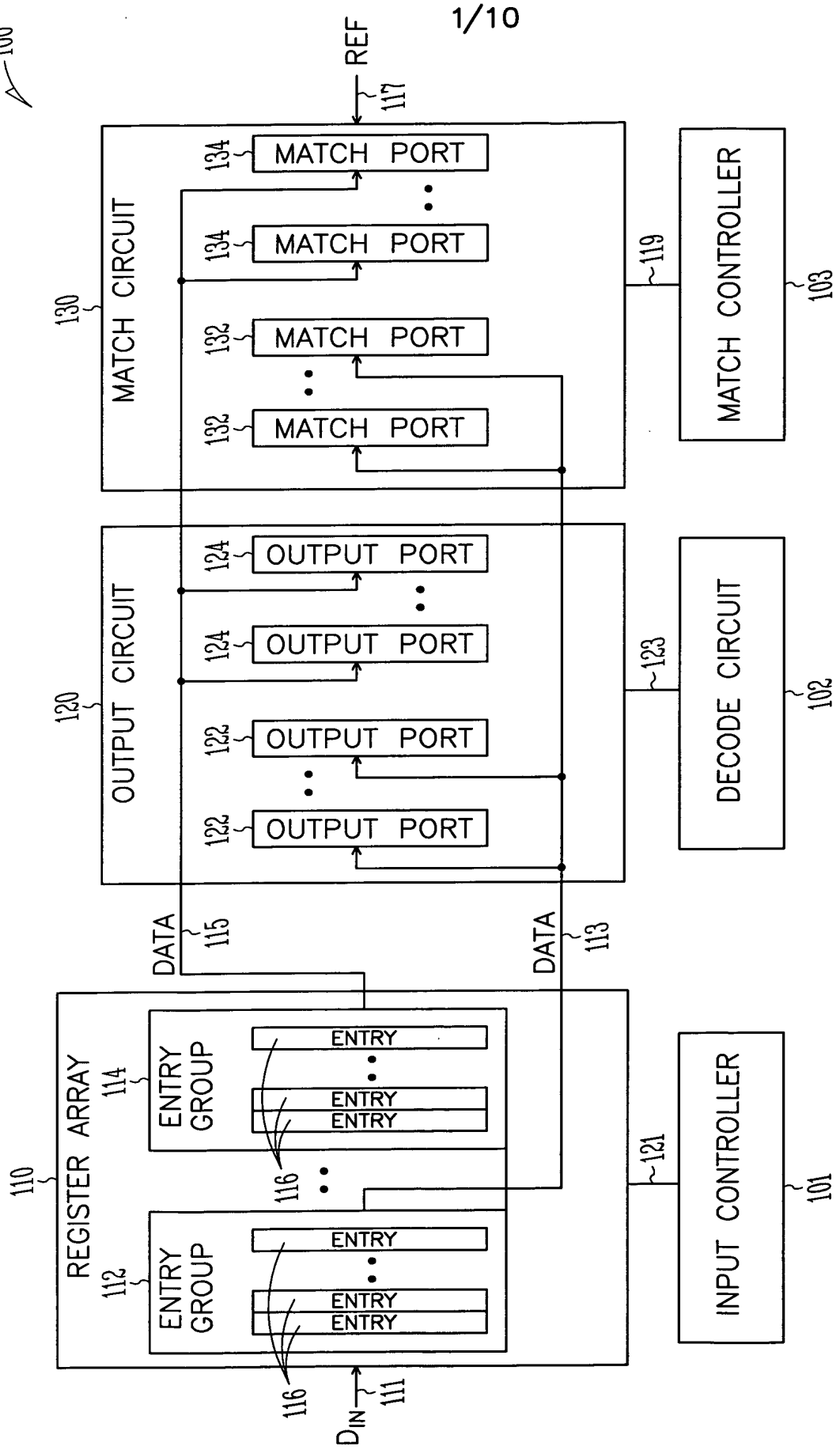


FIG. 1

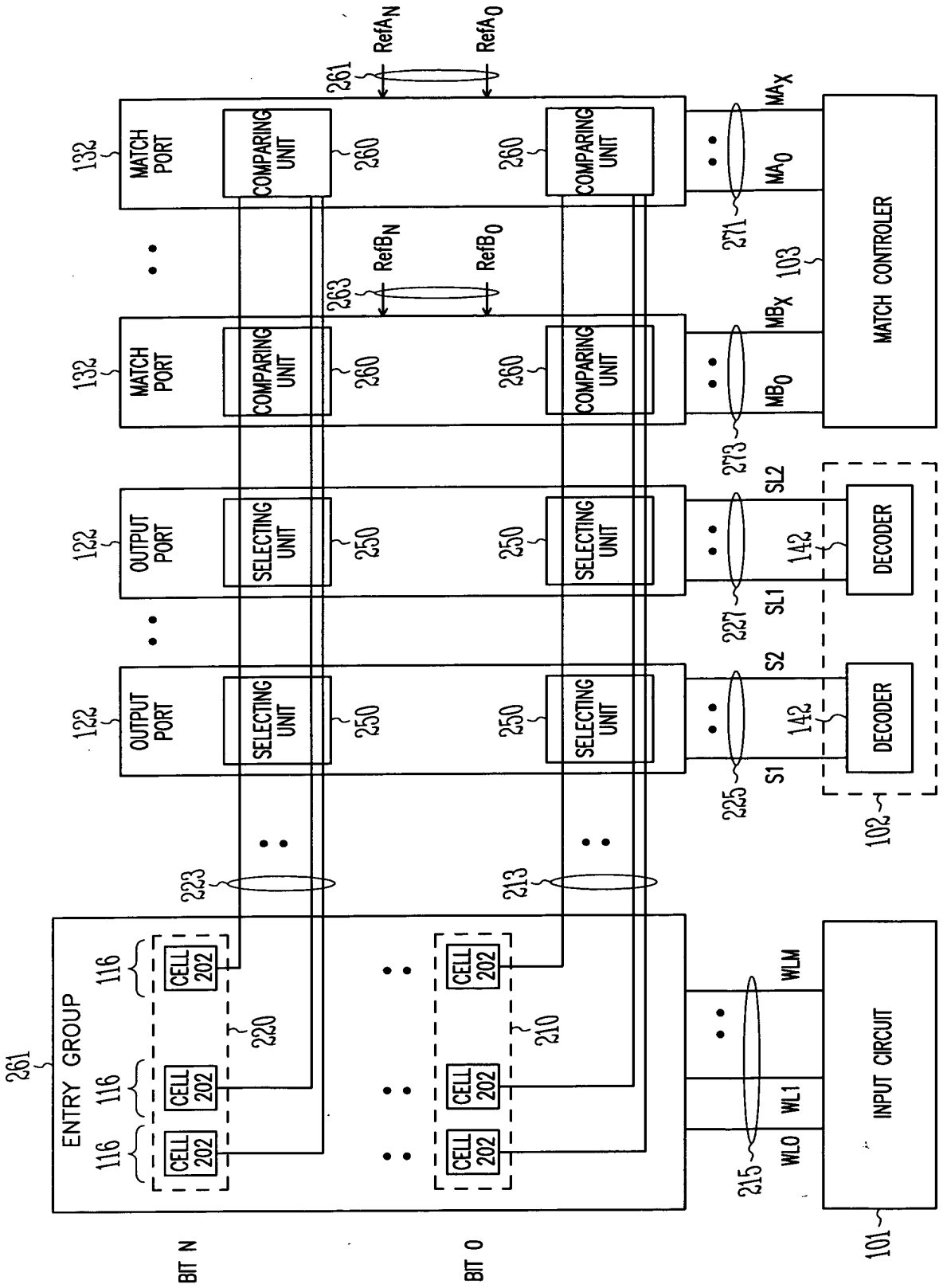

261
RefA_N
RefA_0
132
MATCH PORT
COMPARING UNIT
260
MA_X
MA_0
271
MATCH CONTROLER
103
RefB_N
RefB_0
263
MB_X
MB_0
273
122
OUTPUT PORT
SELECTING UNIT
250
SL2
SL1
227
142
DECODER
S2
S1
225
102
223
213
ENTRY GROUP
116
CELL 202
220
210
WLM
WL1
WL0
215
INPUT CIRCUIT
101
BIT N
BIT 0

FIG. 2

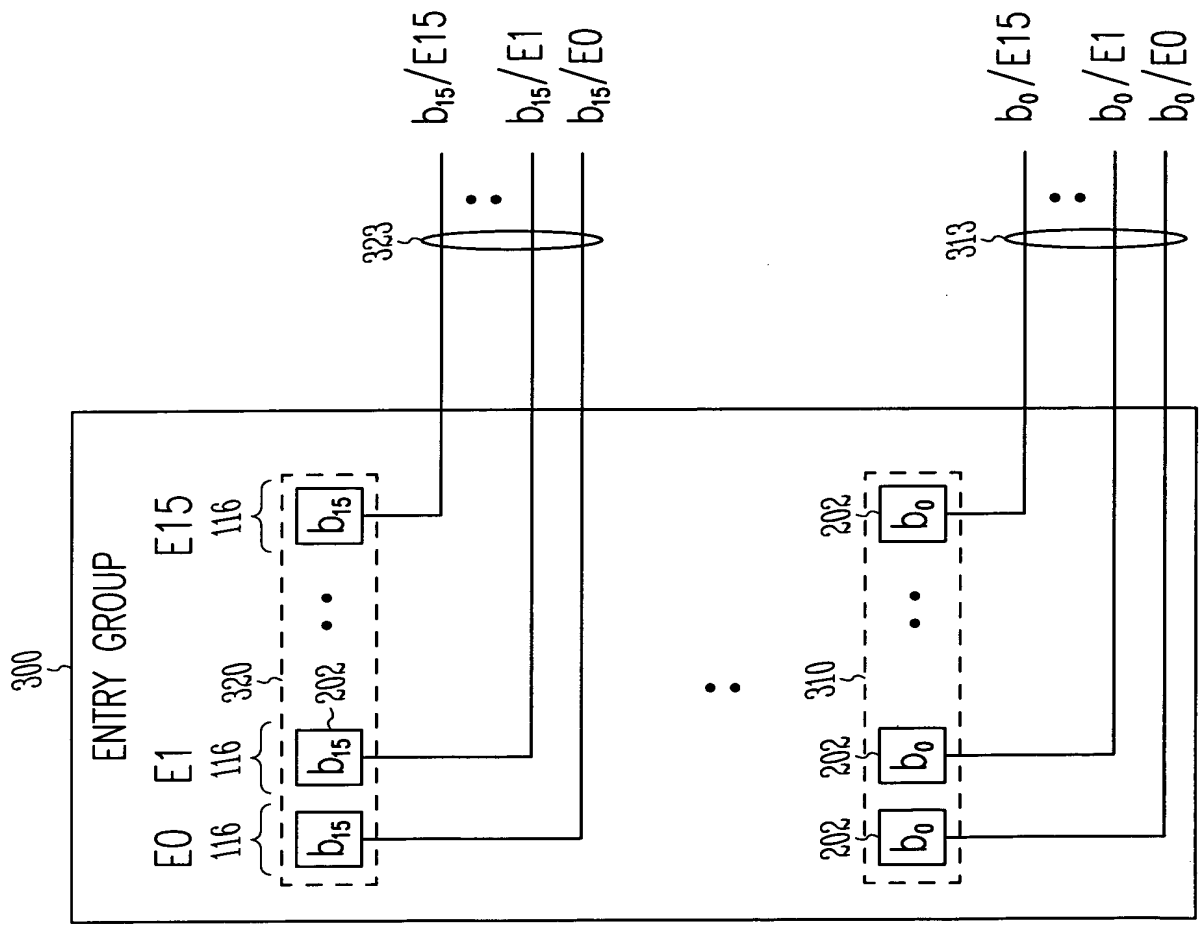

300
ENTRY GROUP
E0
E1
E15
116
320
202
310
323
313
b_{15}/E15
b_{15}/E1
b_{15}/E0
b_0/E15
b_0/E1
b_0/E0
b_{15}
b_0

FIG. 3

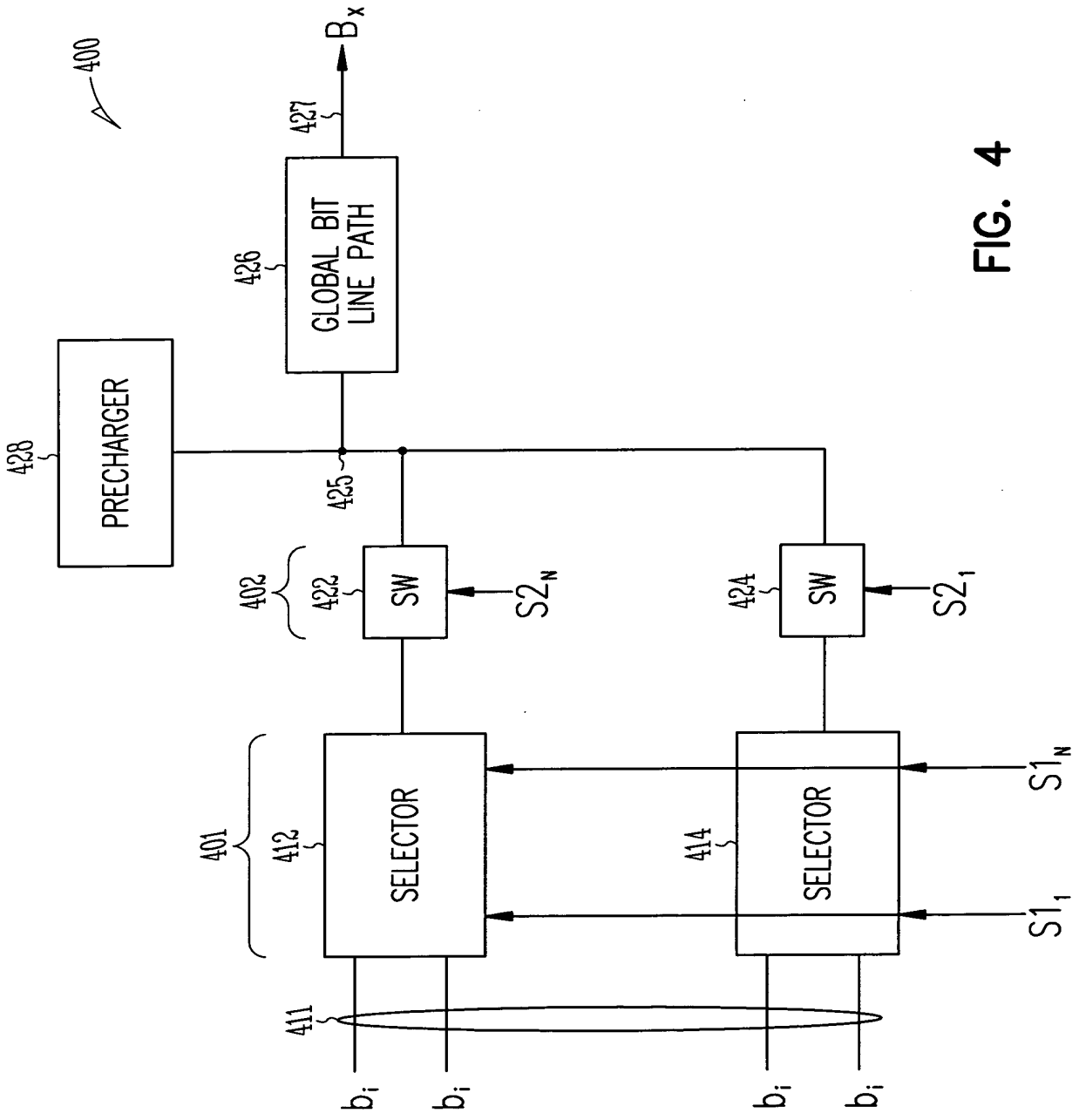

400
B_x
427
GLOBAL BIT LINE PATH
426
PRECHARGER
428
425
402
422
SW
$S2_N$
424
SW
$S2_1$
401
412
SELECTOR
414
SELECTOR
$S1_N$
$S1_1$
411
b_i
b_i
b_i
b_i

FIG. 4

FIG. 5

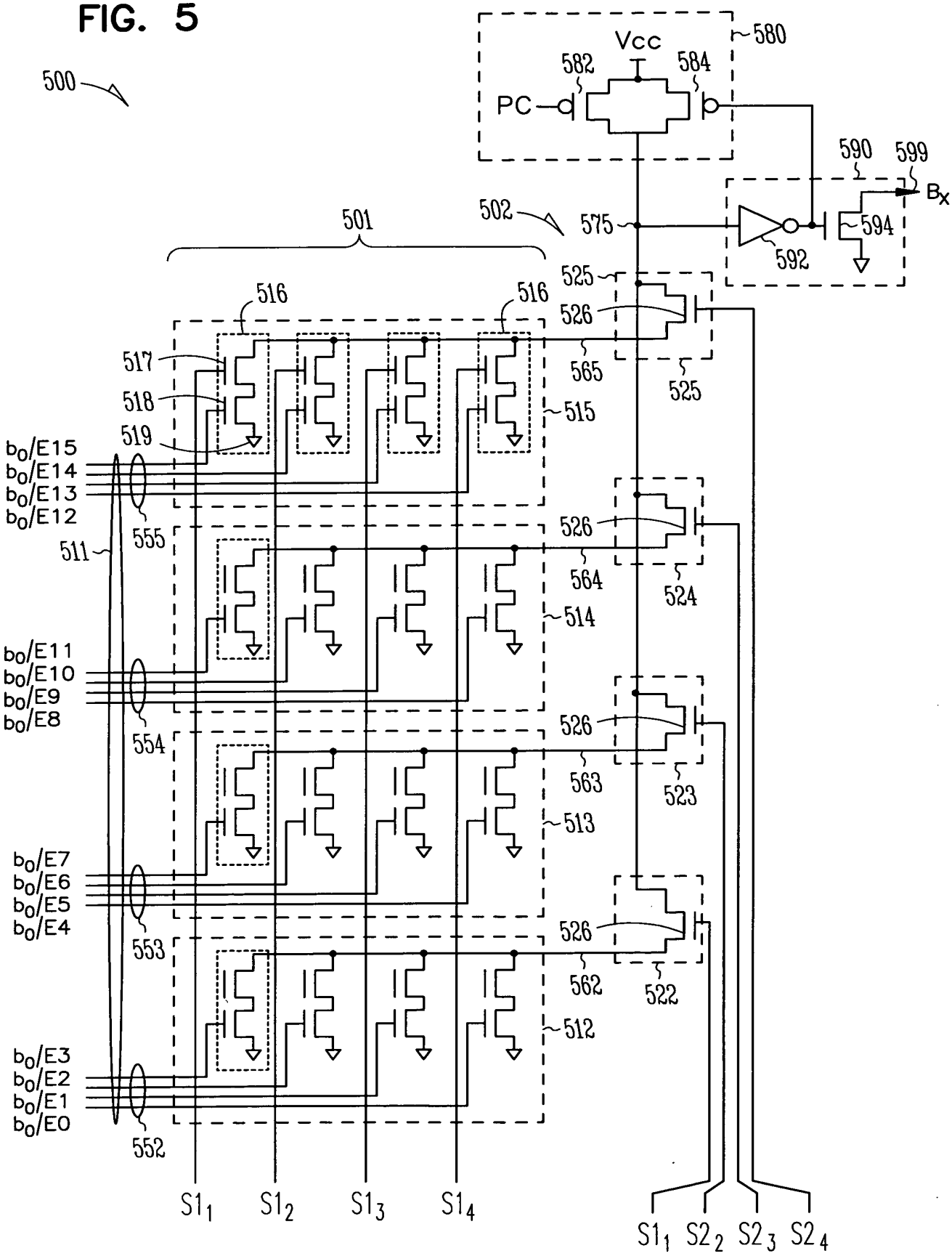
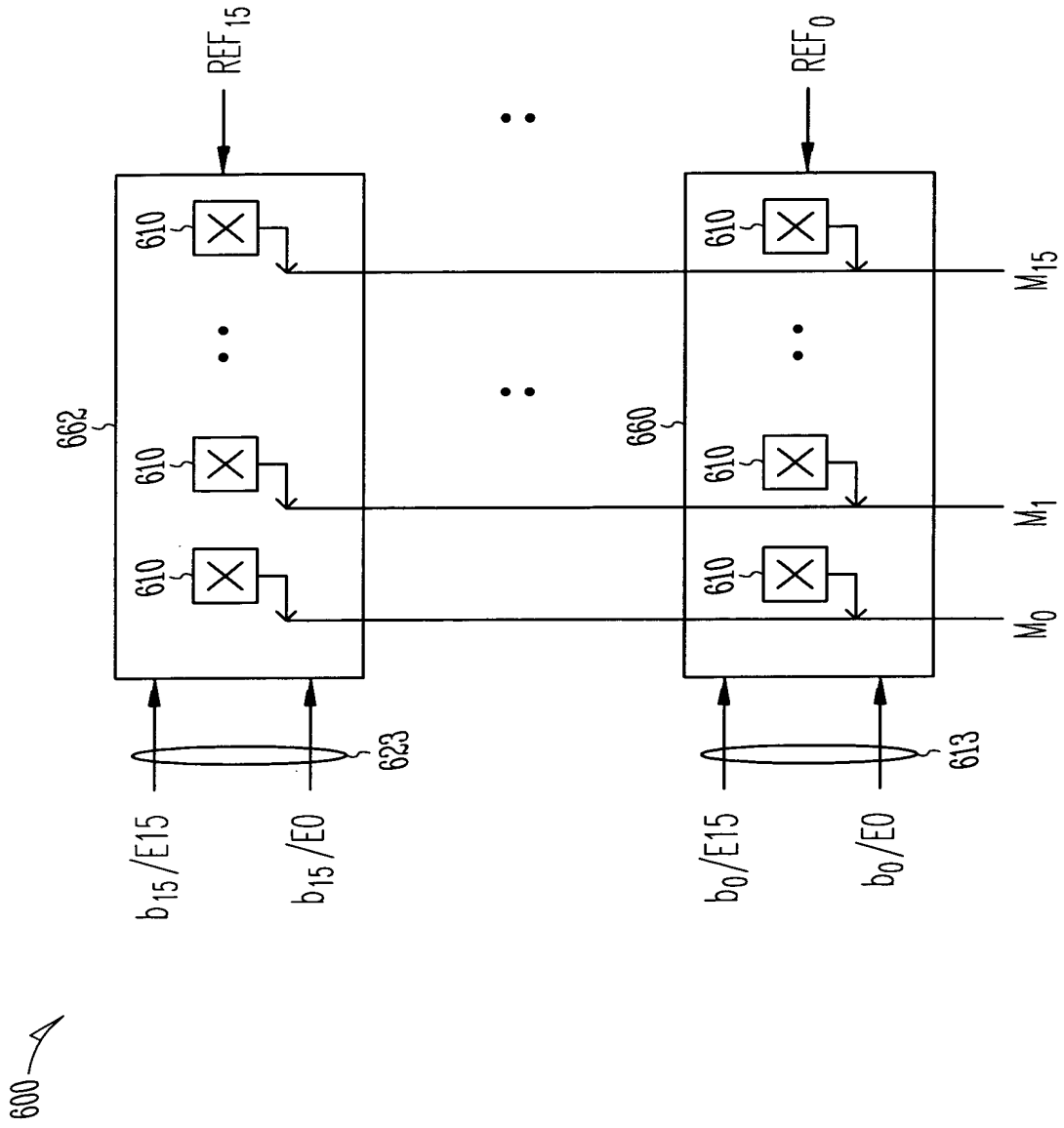

500
501
502
580
Vcc
582
584
PC
590
599
Bx
575
594
592
516
516
517
518
519
515
525
526
565
525
b0/E15
b0/E14
b0/E13
b0/E12
555
511
526
564
524
514
b0/E11
b0/E10
b0/E9
b0/E8
554
526
563
523
513
b0/E7
b0/E6
b0/E5
b0/E4
553
526
562
522
512
b0/E3
b0/E2
b0/E1
b0/E0
552
S1 1
S1 2
S1 3
S1 4
S1 1
S2 2
S2 3
S2 4

FIG. 6


REF15
REF0
610
662
660
M15
M1
M0
623
613
b15/E15
b15/E0
b0/E15
b0/E0
600

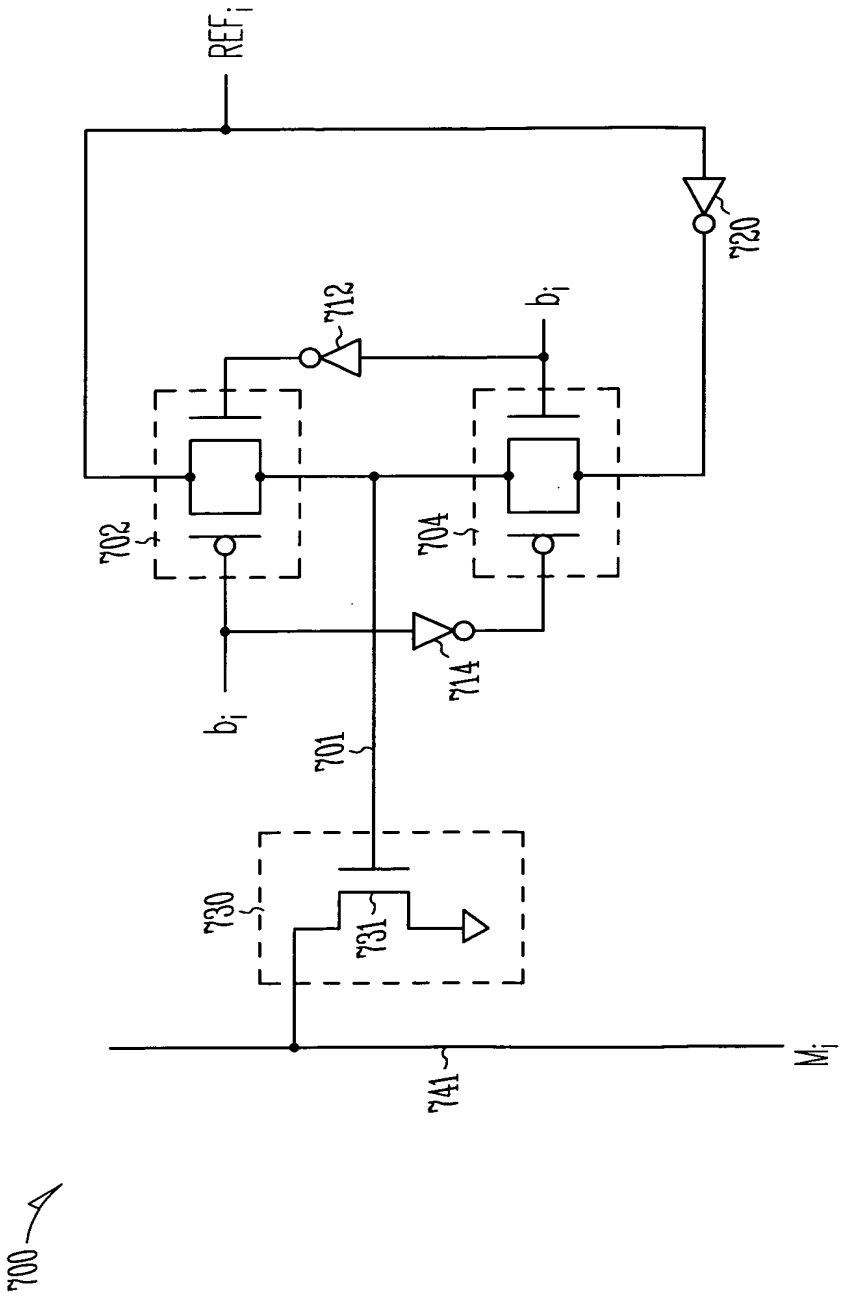


FIG. 7

b_i	REF_i	NODE 701	M_i
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

FIG. 8

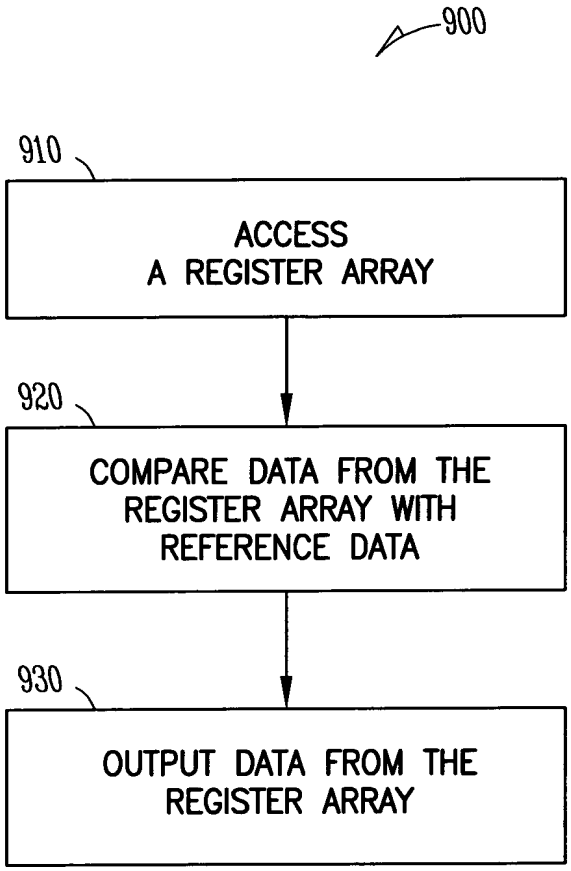

900
910
ACCESS A REGISTER ARRAY
920
COMPARE DATA FROM THE REGISTER ARRAY WITH REFERENCE DATA
930
OUTPUT DATA FROM THE REGISTER ARRAY

FIG. 9

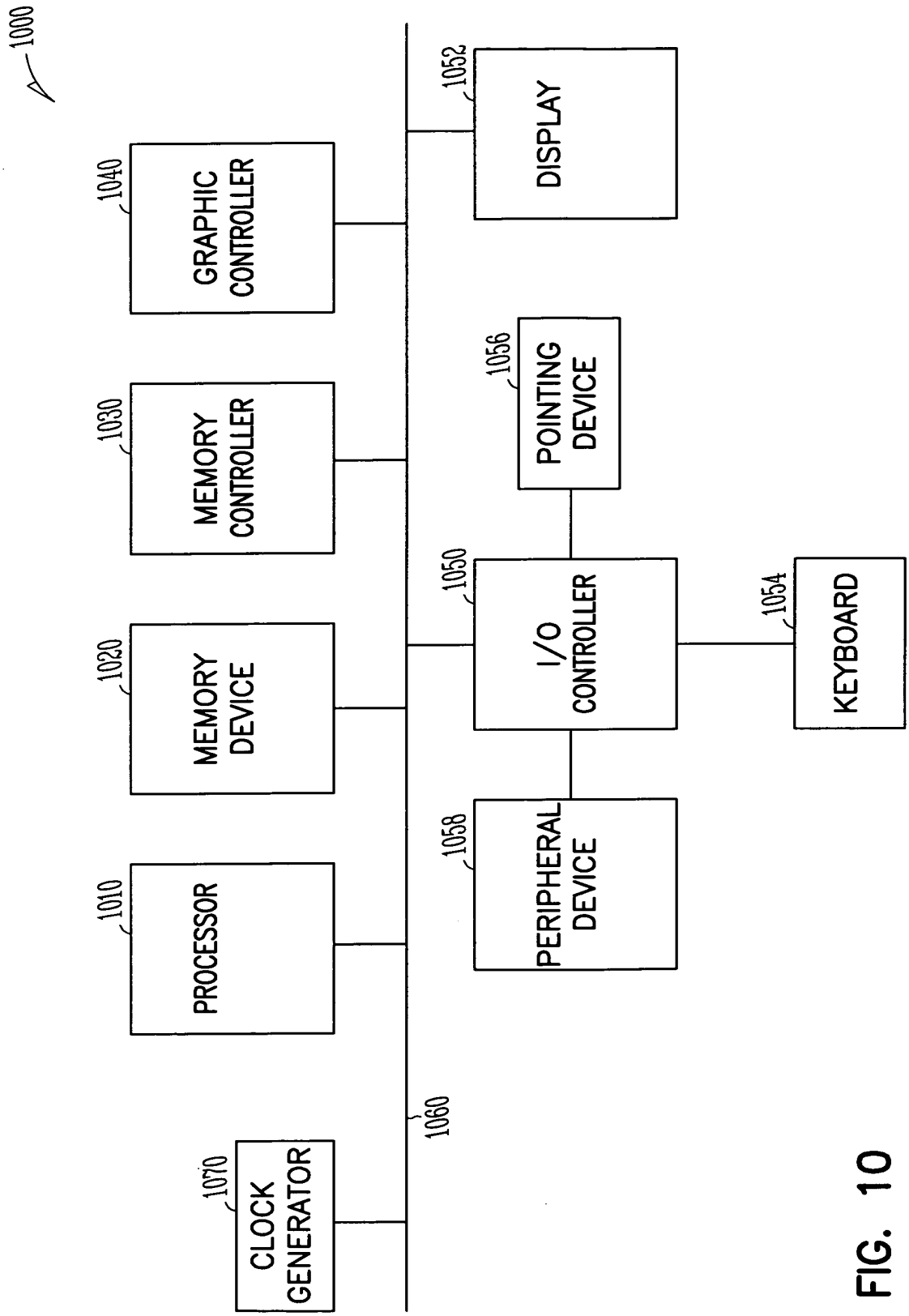

1000
1052
DISPLAY
1040
GRAPHIC CONTROLLER
1056
POINTING DEVICE
1030
MEMORY CONTROLLER
1050
I/O CONTROLLER
1054
KEYBOARD
1020
MEMORY DEVICE
1058
PERIPHERAL DEVICE
1010
PROCESSOR
1060
1070
CLOCK GENERATOR

FIG. 10